NDnano
Notre Dame Nanoscience and Technology

NDnano Summer Undergraduate Research
2023 Project Summary

1. Student name & home university: Yiyang Zhang, Southern University of Science and Technology

2. ND faculty name & department: Ningyuan Cao, Electrical Engineering

3. Summer project title: Universal Programmable Entropy Source for Hyper-Dimensional Computing

4. Briefly describe new skills you acquired during your summer research:

Monte Carlo simulation using HSPICE.
Circuit schematic and layout design & simulation using Cadence Virtuoso.

5. Briefly share a practical application/end use of your research:

Implementation of such universal entropy source could be found in Hyper-Dimensional Computing (HDC), privacy preserving algorithms and machine learning algorithms. My work would greatly reduce the silicon area overhead and power consumption of the entropy generation module while providing programmable results to shorten design time for future HDC circuits.

6. 50- to 75-word abstract of your project:

A topologically symmetric analog entropy generation source has been investigated, boasting small silicon area overhead and power consumption. Uniform, gaussian and gamma distribution can be interchanged via programming supply voltages. Monte-Carlo simulation results utilizing HSPICE meets well with theoretical calculation results from non-linear transformation theory, laying solid foundation for future tape-out verification.

7. References for papers, posters, or presentations of your research:

[1] J. Lee, D. Lee, Y. Lee and Y. Lee, "A 354F2 Leakage-Based Physically Unclonable Function With Lossless Stabilization Through Remapping for Low-Cost IoT Security," in IEEE Journal of Solid-State Circuits, vol. 56, no. 2, pp. 648-657, Feb. 2021, doi: 10.1109/JSSC.2020.3014386.

[2] Z. Zou, Y. Kim, F. Imani, H. Alimohamadi, R. Cammarota and M. Imani, "Scalable Edge-Based Hyperdimensional Learning System with Brain-Like Neural Adaptation," SC21: International Conference for High Performance Computing, Networking, Storage and Analysis, St. Louis, MO, USA, 2021, pp. 1-15, doi: 10.1145/3458817.3480958.

One-page project summary that describes problem, project goal and your activities / results:

Modern machine learning and deep learning algorithms suffers from large time and energy overheads in training of the model. Hyperdimensional computing (HDC) emerged as a promising solution that utilize large hypervectors as computation foundation. Image or object characteristics are being encoded into hypervectors and then going through pre-trained associative search module to match it with optimum results during tasks such as classification.

During the encoding stage of input data, entropy sources that utilize dynamic or static random phenomenon are of great importance. Various proposed HDC schemes in literature have been utilizing entropy sources that provide uniform or gaussian distributions. With this a random projection matrix can be initialized and input vector can be operated with such matrix to produce encoded hypervectors.

For current state of the art works, dedicated ASIC chips have been made with custom entropy generation sources on die. Such solution would take up large silicon area as well as extending the design time thus making it costly. After this summer's effort, a new scheme utilizing intrinsic manufacturing process variations has been designed and simulated to achieve programmable entropy distribution outputs.

The Monte-Carlo simulation is done by utilizing Monte-Carlo and Mismatch library included in TSMC's PDK. Both Spectre and HSPICE have been utilized as the simulator. The simulation results revealed that with the tuning of the supply voltage, all three of uniform, gaussian and gamma distribution outputs could be achieved with the same design with variable input noise configuration. Beside this, a standard deviation tunable design has also been proposed.

During the research, emphasis have been laid on few aspects. First the design is fully in analog domain thus avoiding large digital area overheads. Secondly the design must be electrically symmetric in terms of NMOS & PMOS topology. This indicates that under different operating temperature the design has strong temperature invariance. Third number of transistors utilized must be reduced to minimum to save area as well as lower power consumption.

Upon finishing the simulation and data processing of the above mentioned objectives, the design is ready to enter layout drawing stage and waiting for future tape out opportunities to do physical verification.