NDnano Undergraduate Research Fellowship (NURF)
2015 Project Summary

1. Student name: Rigel Galindo

2. Faculty mentor name: Alan Seabaugh

3. Project title: Nanoelectronics from two-dimensional materials

4. Briefly describe any new skills you acquired during your summer research:

Along this summer I learned how to use Wavevue and Nucleus software to control a Cascade Microtech Semiautomatic Wafer Prober to measure the current-voltage (I-V) characteristics of metal-oxide-semiconductor (MOS) heterostructures. I spent time in the Notre Dame Nanofabrication Facility working in several steps of the fabrication of aluminum oxide gate dielectrics by atomic layer deposition and top contact metallization by electron beam evaporation. Later I tested the devices. I also learned how to handle large amount of data in Matlab and Excel and how to analyze it to produce summary device characteristics. Towards the end of the summer I refined my presentation skills in a talk I gave to other undergraduates and faculty in the NURF program.

5. Briefly share a practical application/end use of your research:

Aluminum oxide is a material that can be used as a back gate oxide. It has a higher relative dielectric constant (9) relative to silicon dioxide (3.9) which means the capacitance of a MOS capacitor is higher for the same geometry. The findings of my summer research helped to characterize the leakage current in Al_2O_3 as function of oxide thickness. This work was aimed to develop thin low leakage back gate oxides for low energy tunneling field effect transistors.

Low leakage gate oxides are needed for the back-gating of two-dimensional (2D) crystal materials. For example, atomically thin tungsten diselenide (WSe_2) is being explored for use as a transistor channel. The gate oxide serves as the dielectric layer separating the gate from the channel. The gate controls the channel charge, which is directly proportional to the electric field in the oxide. Gate oxides made of high-κ dielectric materials achieve higher capacitance thus increase the charge in the channel.

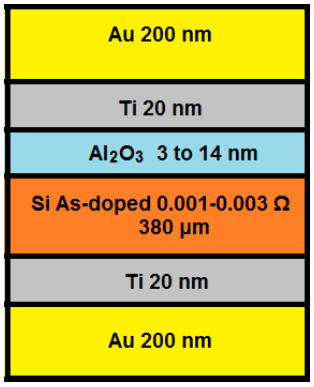

Figure 1 Structure of the devices tested.

To get an understanding of what I-V characteristic to expect I used Matlab to plot the formula of Simmons's contained in the paper *Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film*. In the clean room the first fabrication step was to clean the wafers, after that my grad student advisor Mina Asghari helped me to produce the oxide by atomic layer deposition (ALD). I deposited thousands of micrometric contacts on each wafer using electron beam evaporators. Once the samples were ready measurements were taken with the Cascade semiautomatic prober. The objective was to compare Simmons's plots with the experimental data. Traces of the I-V measurements were made on Matlab as well as cumulative distribution plots. Some of the findings were that the contacts were very sensitive to the probes pressure which can damage the oxide and causes early breakdown. Another finding was the high uniformity of the metal-oxide-semiconductor fabrication process

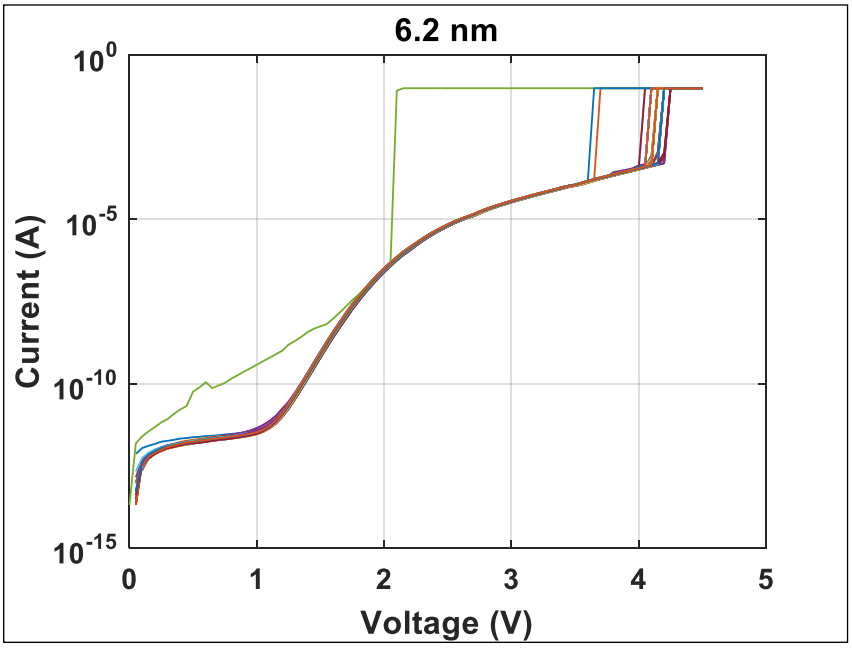

Figure 2 I-V plot for 100 devices containing a 6.2 nm thick aluminum oxide in a metal-oxide-semiconductor structure on n-type Si.