ND*nano* Undergraduate Research Fellowship (NURF)
2014 Project Summary

1. Student name: Rene Celis Cordova

2. Faculty mentor name: Dr. Gregory Snider

3. Project title: Ultra-Low Energy Microprocessor Design

4. Briefly describe any new skills you acquired during your summer research:

This summer was my first real research experience, therefore I got to learn many new skills. First of all I worked inside a cleanroom for the first time, and I learned about CMOS processing and testing. I was able to perform several standard photolithography steps on a silicon wafer, and in the end I acquired very valuable experience in on-wafer testing. For example, I learned how to use a probe card to test several signals simultaneously on a probe station. And by the end of the summer, having to design a new microprocessor, I also acquired strong chip design skills.

5. Briefly share a practical application/end use of your research:

Power consumption in electronic devices represents a major problem nowadays. Everybody that owns a laptop has seen the effects of heat dissipation, and how energy dissipated by electronic devices can even burn our skin. On the other side the industry is held back by this very same problem; computers are not as fast or small as they could be due to heat dissipation. The research I performed during the summer tries to solve this problem, by creating a microprocessor that could dissipate much less energy than the current implementations.

Project summary:

My main contribution to the project was in chip design, more specifically in a new type of microprocessor. While current microprocessors use standard CMOS devices and computation technologies, the new design uses adiabatic computation to recycle energy. This new computation method uses ramping clocks to power the integrated circuit. Where the power clocks have adiabatic, or slow relative to RC time constants, changes between three different states: VDD, VSS, and GND. Charging and discharging the transistors in an adiabatic way, combined with reversible logic can avoid the dissipation of energy, since dissipation is only necessary when information is erased.

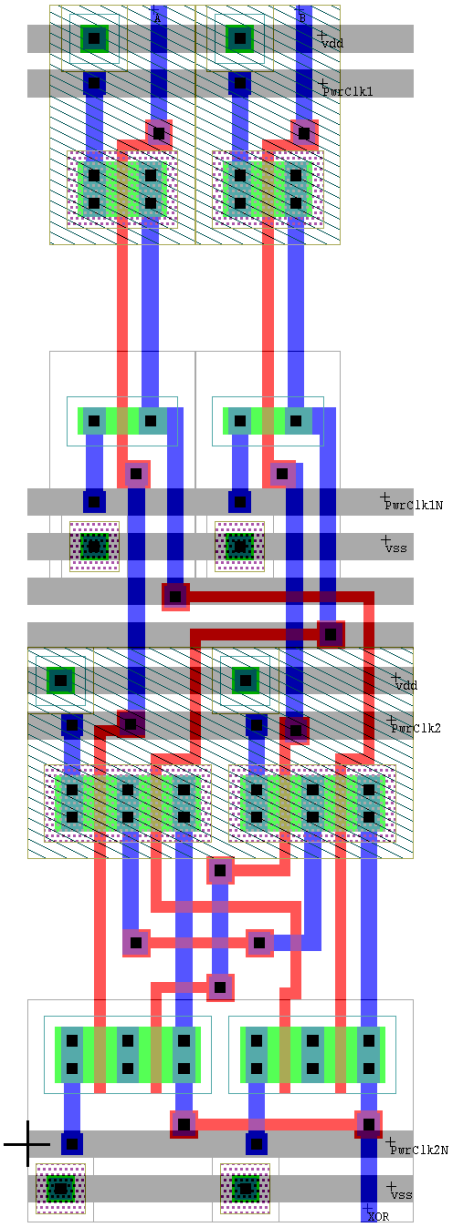


Figure 1: XOR standard cell layout, implemented using reversible logic and two different pairs of adiabatic power clocks (PwrClk1 and PwrClk2).

The chip was designed as a full-custom layout based on standard cells. As it can be seen in Figure 1, two pairs of adiabatic clocks power different gates which creates reversible logic for the adiabatic computation. This implementation represents a more efficient microprocessor that dissipates much less energy than current devices. It should be noted that adiabatic clocking is only slow relative to the maximum transistor speed. Microprocessors already operate at frequencies well below the maximum due to power constraints.

Publications (papers/posters/presentations):

- Summer Undergraduate Research Symposium 2014, Poster presentation

Ultra-Low Energy Microprocessor Design

Rene Celis-Cordova[12], Cesar O. Campos-Aguillon[12], Ismo K. Hanninen[13], and Gregory L. Snider[1]*

[1] Department of Electrical Engineering, University of Notre Dame

[2] Department of Electrical and Computer Engineering, Tecnologico de Monterrey, Mexico

[3] Department of Computer Systems, Tampere University of Technology, Finland

**Correspondence author. Email address: renecelis22@hotmail.com*

In the current microelectronic industry power dissipation and the associated heat produced by devices represents a major problem. Modern microprocessors dissipate energy as heat, and this heat already limits their speed and packing density. However, studies have shown that more efficient devices are possible by changing the traditional computation method to one with lower energy dissipation.

This research presents a novel approach for an energy efficient microprocessor. While current microprocessors use standard CMOS devices and computation technologies, the proposed design uses adiabatic computation to recycle energy. This new computation method uses ramping clocks to power the integrated circuit. These power clocks have adiabatic, or slow relative to RC time constants, changes between three different states. Charging and discharging the transistors in an adiabatic way, combined with reversible logic can avoid the dissipation of energy, since dissipation is only necessary when information is erased. This creates a more efficient microprocessor that dissipates much less energy than current devices. It should be noted that adiabatic clocking is only slow relative to the maximum transistor speed. Microprocessors already operate at frequencies well below the maximum due to power constraints.

The final design consists of a complete semiconductor layout for an 8-bit MIPS microprocessor using adiabatic power clocks. The microarchitecture implemented is a multicycle non-pipeline RISC processor which supports a set of 10 different instructions. The entire microprocessor design is compatible with a standard CMOS fabrication process, therefore it will be fabricated using two different technologies: the Notre Dame 1.5um process, and the Mosis 0.5um C5 process. The design represents the first microprocessor of its kind.

Poster:

Ultra-Low Energy Microprocessor Design

Rene Celis-Cordova[12], Cesar O. Campos-Aguillon[12], Ismo K. Hanninen[13], and Gregory L. Snider[1]

[1] Department of Electrical Engineering, University of Notre Dame
[2] Department of Electrical and Computer Engineering, Tecnologico de Monterrey, Mexico
[3] Department of Computer Systems, Tampere University of Technology, Finland

Why Ultra-Low Energy?

In the current electronic industry power dissipation and the associated heat produced by devices represents a major problem. Modern microprocessors dissipate energy as heat, and this heat already limits their speed and packing density.

More efficient devices are possible by changing the traditional computation method to one with lower energy dissipation. [1]

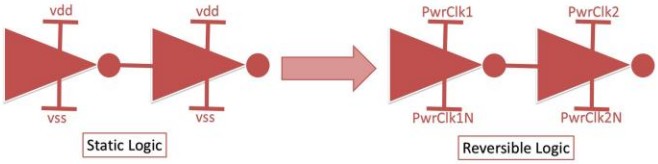
This research presents a novel approach for an energy efficient microprocessor that uses adiabatic computation to recycle energy.

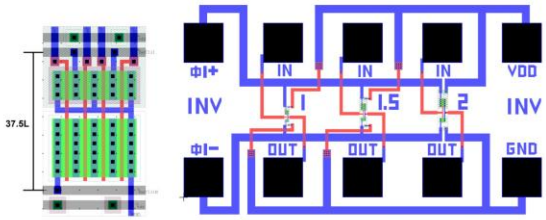
Background

The new microprocessor design uses ramping clocks to power the integrated circuit. These power clocks have adiabatic, or slow relative to RC time constants, changes between three different states. Charging and discharging the transistors in an adiabatic way, combined with reversible logic can avoid the dissipation of energy, since dissipation is only necessary when information is erased. [1,3]

Methodology

The entire microprocessor design is compatible with a standard CMOS fabrication process, therefore it will be fabricated using two different technologies: the Notre Dame 1.5um process, and the Mosis 0.5um C5 process. The reversible logic can be created by transforming the static CMOS well-known circuit architecture.

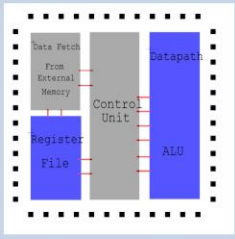




The layout follows the concept of a standard cell, where L is the minimum gate length. Test circuits can be fabricated in different sizes, such as 1um, 1.5um and 2um.

Results

The final design consists of a complete semiconductor layout for an 8-bit MIPS microprocessor using adiabatic power clocks. The microarchitecture implemented is a multicycle non-pipeline RISC processor which supports a set of 10 different instructions. [2]



Conclusion

This design represents the first microprocessor of its kind. It shows that adiabatic computation is possible and a viable option to solve the current heat dissipation problem.

It should be noted that adiabatic clocking is only slow relative to the maximum transistor speed. Microprocessors already operate at frequencies well below the maximum due to power constraints.

References

[1] A. O. Orlov, C. S. Lent, C. C. Thorpe, G. P. Boechler, and G. L. Snider: Jpn. J. Appl. Phys. 51 (2012)
[2] D. Harris & S. Harris, "Digital Design and Computer Architecture," San Francisco, CA: Morgan Kaufmann, 2007.
[3] G. P. Boechler, J. M. Whitney, C. S. Lent, A. O. Orlov, and G. L. Snider: Appl. Phys. Lett. 97 (2010) 103502