ND*nano* Undergraduate Research Fellowship (NURF)
2013 Project Summary

1) Student name: Shoubhik Gupta
2) Faculty mentor name: Dr. Debdeep Jena and Dr. Huili (Grace) Xing
3) Project title: 2-dimensional semiconductors: New toys for the next nano(opto) electronic era

4) Briefly describe any new skills you acquired during your summer research:

i) I have gained hands-on experience on the fabrication of nano-scale devices in the cleanroom.

ii) I Learnt the use of software tools such as Mathematica for modeling and L-Edit for device layout.

iii) I learnt to use Cascade 11000 Probe Station and IPE Probe Station for the electrical characterization of fabricated transistor devices.

5) Please briefly share a practical application/end use of your research:

Two-dimensional (2D) materials, such as molybdenum disulfide (MoS_2), have been shown to exhibit excellent electrical and optical properties. They overcome the shortcoming of zero band-gap graphene. The lack of band-gap in graphene has limited its use as a switching device in digital electronics. Monolayer MoS_2 has band gap varying between 1.8 eV in single layer to 1.3 eV in bulk. It has recently been used in field effect transistors with excellent gate modulation and current pinch-off. The exfoliated thin MoS_2 on SiO_2 devices have demonstrated field-effect operation with high on-off ratios at room temperature. These MoS_2 FETs offer a new possibility of using them in low power switching devices.

Project summary:

Fabrication: The fabrication of MoS_2 FETs starts with the exfoliation of MoS_2 thin films by micro-mechanical cleavage technique using scotch tape from commercially available bulk MoS_2 crystals. The scotch tape with ultrathin crystals is pressed against the surface of a substrate composed of degenerately doped Si with 285nm of SiO_2. The substrate is imaged using an optical microscope equipped with a color camera.

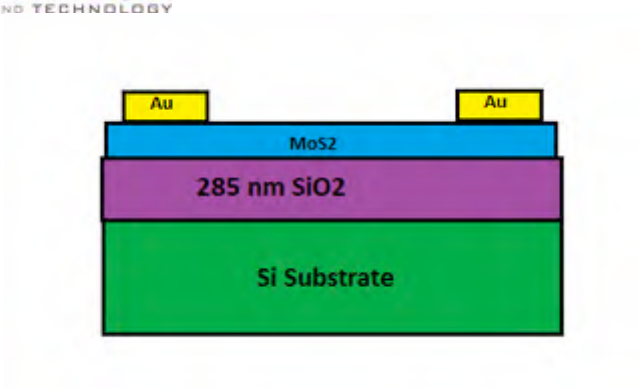

Fig.1: The device geometry of a back-gated MoS2 FET with W/L = ½ um

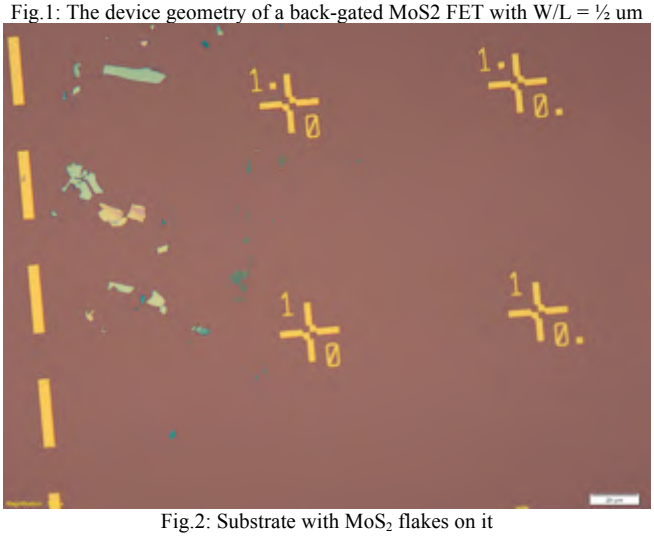

Fig.2: Substrate with MoS_2 flakes on it

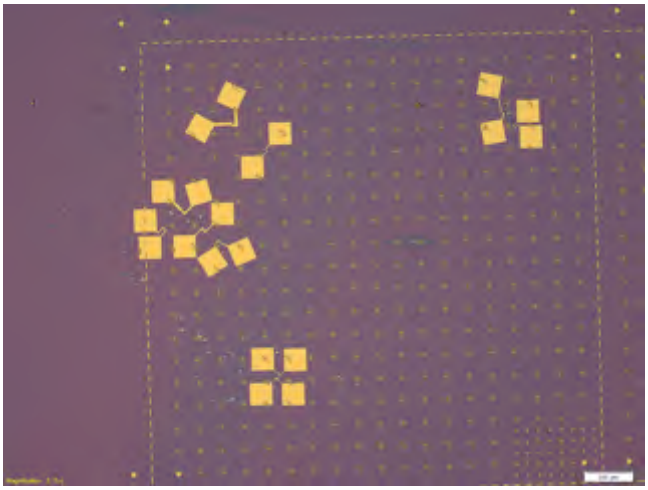

Fig.3: Fabricated devices

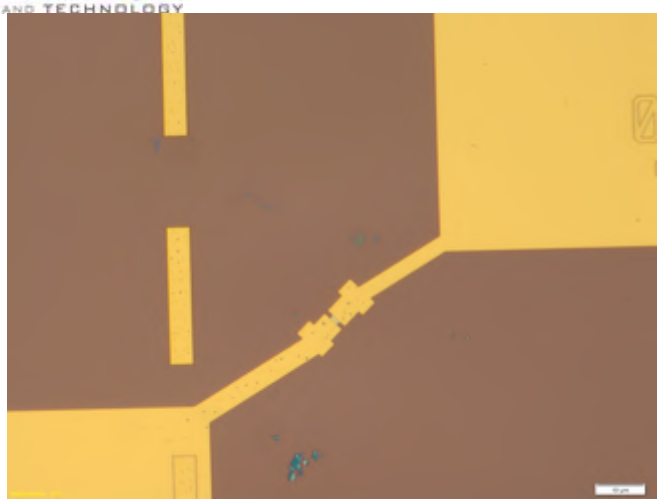

Fig.4: : Optical image of a typical PMMA-supported MoS_2 device. The green area is the MoS_2 flake, yellow areas are Au electrodes. The brown area is the PMMA/SiO_2/Si substrate

Single layers of MoS_2 are located with respect to align markers. Because of their optical contrast monolayers can be easily identified (violet color). After identifying the monolayers of MoS_2, images are taken and the Source-Drain contacts were designed using L-Edit Software. Samples are coated with MMA and baked at 170 °C for 3 min. Then they are coated with PMMA and exposed using an electron-beam lithography system. MIBK solution is used as a developer which removes the parts of the resist exposed to the E-Beam. After development in MIBK, we evaporate Au as the contact materials and lift-off in acetone. We anneal the devices in a vacuum tube furnace with temperature of 200 °C. Device measurements are performed using a Cascade 11000 probe station.

Modeling of Device: The drift-diffusion model for single-layer transition metal dichalcogenide field-effect transistors is used to calculate the current-voltage characteristics of the MoS_2 FETs. The only unknown input parameters to the model are the carrier mobility, and the contact resistance.

.

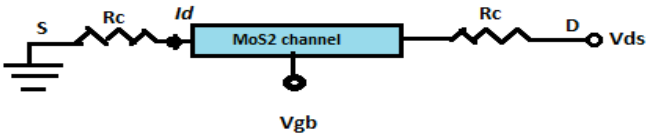

Fig.5: An equivalent circuit model for the MoS_2 TFT including the effect of the contact resistance, Rc

At high positive gate biases, the channel is flooded with accumulated carriers and is highly conductive, and the contact resistances limit the current. The measured gate and drain voltages are not those of the intrinsic device, but are higher due to potential drops at the source and drain contact resistances, as shown in Fig 5. The actual external voltages are thus given by

$Vgs\_ext = Vgs\_\text{int} + Id*Rs$, and

$Vds\_ext = Vds\_\text{int} + Id*(Rs + Rs)$.

We use *Rs* = *Rd* = *Rc* as the contact resistance for the evaluation. Due to the small size of the MoS_2 flakes, we cannot use TLM for extracting the value of contact resistance. But the value is easily obtained at a high gate bias, since under that condition the channel resistance is negligible, and the net resistance is *Vds* / *ID* = 2*Rc* . The best fit to experimental data has been obtained at Rc = 100 kohm-um and an electron mobility = 313 cm^2/V-s. Figs 6 and 7 show the final results.

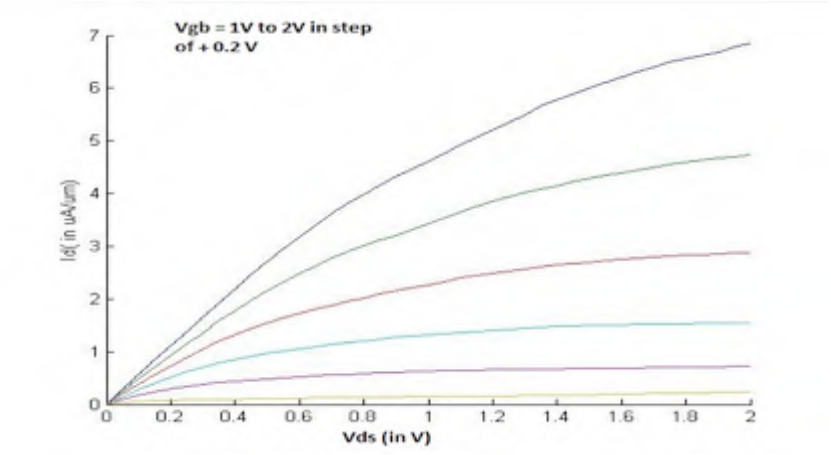

Fig.6: MoS2 device characteristic curves

The experimentally measured transistor characteristics are shown in Fig 6, and Fig 7 shows the fit to the model, which is reasonable.

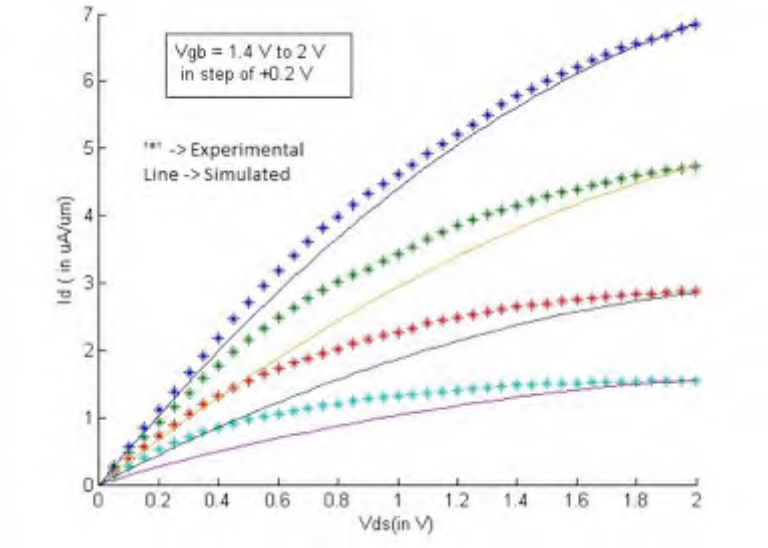

Fig.7: Measured (* line) and simulated (- line) behavior of MoS_2 FETs taking into account the effect of contact resistance.