

Nanoelectronics Undergraduate Research Fellowship (NURF) 2010 Project Summary

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Project title: Energy efficient tunnel transistor technology

With advantages of low subthreshold swing and low off-state leakage current, TFETs (tunnel field-effect transistors) are becoming a promising area of research in electronic devices. To develop working devices, we have three approaches, namely nanowire TFET (in collaboration with Penn State University), lateral TFET, and vertical TFET. Scaled drawings of the processes are therefore needed for group discussions and publications.

My main contribution towards the project involves creating and revising the drawings using Adobe Illustrator. With experimental data from other researchers and design specifications from fabrication recipes, I was able to draw to scale an Illustrator file for each of the processes, showing all the detailed layer descriptions. These files offer a better visual and mental image of the processes under development and facilitate future publications and patent applications.

Posters:

Vertical and Lateral Tunnel FET Processes

Nanowire Tunnel Junction Process for Tunnel FETs