# NDnano Undergraduate Research Fellowship (NURF)
# 2015 Project Summary

**1. Student name:** Sergio Alberto Dieck Sa

**2. Faculty mentor name:** Dr. Gregory Snider

**3. Project title:** Ultra-Low Energy Computation

**4. Briefly describe any new skills you acquired during your summer research:**

Participating in the NURF program was my first research experience. I had the opportunity to work inside a cleanroom where I performed different tasks involved in integrated circuit fabrication such as carrying out basic photolithography steps or performing several tests on the silicon wafers. I acquired new layout design skills since we worked on adiabatic circuits during the summer such as designing a 3-bit shift register, a 4-bit counter and an ALU (Arithmetic Logic Unit) working with 20nm process technology. I improved my programming skills during the design of a logic analyzer to perform certain measurements that the probe station couldn't achieve; for example testing whether or not the Flip-Flops were working correctly.

**5. Briefly share a practical application/end use of your research:**

Nowadays, one of the major problems in the microelectronics industry is power dissipation and its associated heat generation. Companies such as Microsoft and Sony have suffered from this problem; the overheating and failure of their videogame consoles has caused negative impacts on the industry's sales. Recycling the energy used in computation will reduce the power consumption of many electronic devices such as cellphones causing battery life last longer. The research I performed this summer was focused in exploring the limits of ultra-low power computing, and designing, building and measuring circuits that test these limits.
We designed adiabatic circuits in a 20nm process technology to reduce power consumption and heat dissipation in a smaller scale than past implementations.

**Project Summary:**

My main contribution to the research was the fabrication of a logic analyzer and the design of a software interface that could control seven waveform generators to produce the Bennett Clocks. First of all, the main concern was that we couldn't test some of the components of an adiabatic processor since the probe station that is currently in the clean room doesn't have the capability of performing logic tests. I programmed a DAQ (Data Acquisition) system called "Labjack" that takes an excel file as input which defines the input and output pins and their corresponding output value. After loading the excel file, the program writes the results of the test to another excel file where you can easily analyze results. This system can be used to do simple functional tests of circuits. More sophisticated testing requires arbitrary waveform generators to produce the specific waveforms needed for Bennett clocking. To charge and discharge the transistors in an adiabatic way, ramping clocks known as Bennett clocks are used to power the integrated circuits. The software interface was made to control seven waveform generators that

could produce a certain number of Bennett clocks depending on the number of phases needed. By powering the circuits this way and implementing reversible logic, we are able to avoid the dissipation of energy by recycling it instead, since Landauer's principle states that dissipation occurs only when information is destroyed.

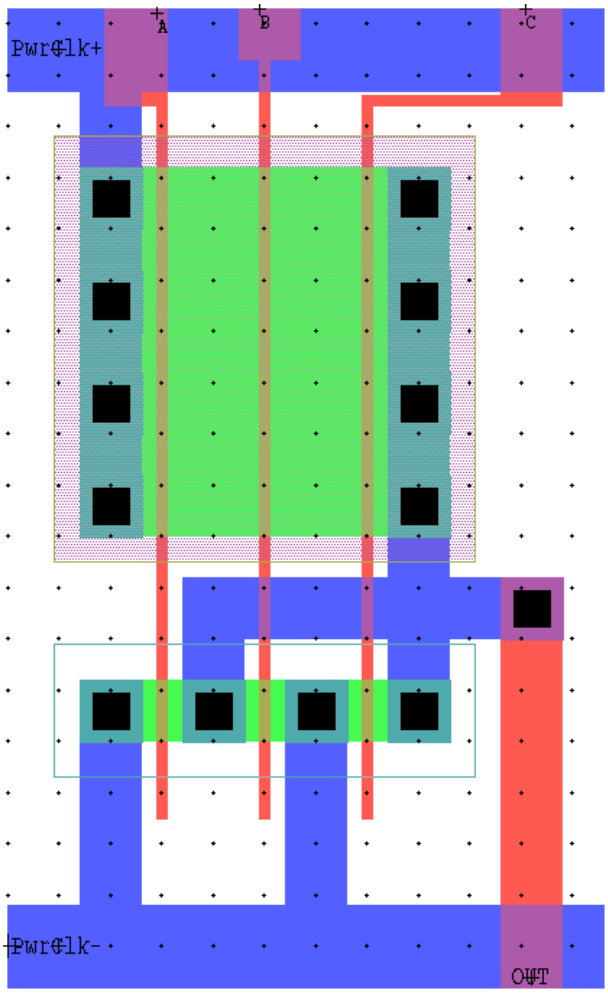


Figure 1: *3-Input NOR standard cell layout, FDSOI 20nm design implementing reversible logic and a pair of adiabatic power clocks (PwrCLK+ and PwrCLK-)*

In addition, I had the opportunity to design some adiabatic circuits working with FDSOI (Fully Depleted Silicon On Insulator) 20nm process. The design rules we used when working with this technology differed from previous layouts creating a substantial challenge for us. This is because we could only use Metal 1, requiring more space than needed in a 2-layer metal design. The huge advantage of this FDSOI process is that there is no need for p and n wells for the transistors. Due to this, VDD and VSS rails were no longer necessary, reducing circuit size. Figure 1 represents an implementation of a 3 Input NOR layout design using FDSOI 20nm process where it can be observed that the only power supply used are the adiabatic clocks achieving less energy dissipation than traditional CMOS NOR devices.