ND*nano* Undergraduate Research Fellowship (NURF)
2012 Project Summary

1) Student name: Joshua Vahala
2) Faculty mentor name: Alan Seabaugh, Susan Fullerton
3) Project title: Electrical characterization of ion transport in planar graphene/PEO:$LiClO_4$/graphene structures

4) Briefly describe any new skills you acquired during your summer research: I have learned to take and interpret current-voltage *(I-V)* measurements while gaining the ability to configure new measurements as needed. Also, I have become highly capable with OriginLab data analysis software and learned how to model electrochemical transport using COMSOL Multiphysics software.

5) Please briefly share a practical application/end use of your research: This research could be used for low voltage, analog and digital logic and memory. The results from scanning the backgate voltage with a constant source-drain potential suggests a capability to store more than one bit, unlike a traditional transistor.

Project summary:

A single atomic layer of carbon represents graphene, and this material, unlike its multi-layered relative graphite, presents itself to a surfeit of possibilities for electronic applications due to its high conductivity, light weight, flexibility, and ability to act as a semiconductor when formed into a ribbon at the nanometer scale. Also, because of its two-dimensional characteristics, an ion interacting with its surface greatly affects the properties of the material. This research investigated the effect of a solid polymer electrolyte between the 2D edges of graphene when supplied with an electric potential to induce an interaction. The solid polymer electrolyte we used was polyethylene oxide (PEO). Lithium (Li+) and perchlorate ions (ClO_4-) were incorporated into the PEO to provide ion conductivity. By collaborating with concurrent research on the electric characterization of graphene surfaces by NURF student Samuel Leung, a broad understanding of the solid polymer electrolyte/graphene model was generated.

Using a B1500 Semiconductor Device Analyzer along with a microprobe station, *I-V* tests were performed on the device shown in Figure 1.

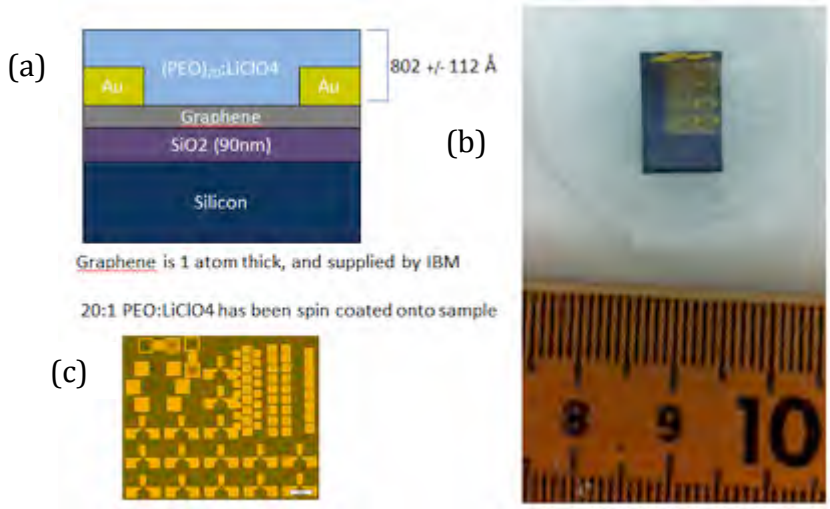

Figure 1. (a) Simplified cross-section of the graphene test structure characterized in this project, (b) Entire IBM14 wafer with scale in cm, (c) 1/12 of wafer shown in (b) showing individual transistors

The most revealing tests came from measurements with a gap between graphene edges (Figure 1(a) shows the cross-section without the gap) . By applying a constant potential (100mV) across the gap, an electric field is created in the graphene gap to drive an ion current in the PEO. By varying the backgate voltage from negative to positive biases, we expect that the graphene electrodes are tuned between hole and electron rich conductivities respectively. If holes are induced in the graphene, then ClO_4- ions should more preferentially react with the graphene to give up its electron. Alternately, if electrons are induced in the graphene, then Li+ ions should react with the graphene to take an electron. In either process, current is generated due to ion transfer. This test is demonstrated in Figure 2 on a 2 micron gap and a 16 micron gap with a 100mV source-drain voltage, and a -20 to 20V backgate double scan at 200 mV/s.

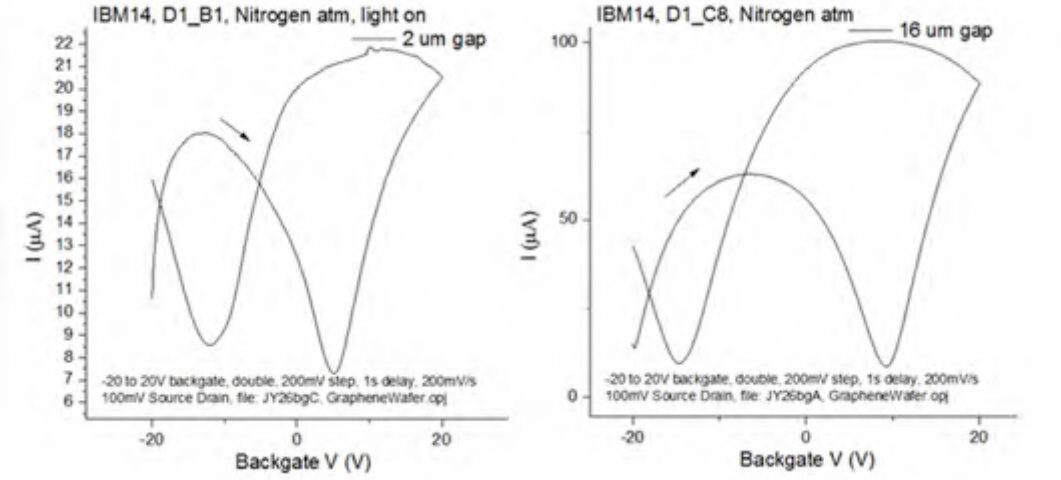

Figure 2. When electrons are induced (positive back-gate voltage), Li+ ions supply more current to system than when holes are induced in graphene

As shown in Figure 2, the magnitude of the current between the graphene electrodes is based on where on the plot the point is and has been. That is, some values can only be achieved

under the condition that you are on the reverse sweep and not the forward sweep (i.e. 20 μA current on the 2 μm gap can only be found on the reverse sweep). This interesting phenomenon (the curve was not expected to open an envelope) suggests the device could be used for multi-bit storage because the present state would be dependent on the previous state. This device could usher in a new form of transistor that introduces both memory and logic functionality in a single device.

Publications (papers/posters/presentations):

I gave weekly presentations of my progress in group meetings.