ND*nano* Undergraduate Research Fellowship (NURF)
2013 Project Summary

1) Student name: Dillon Bak
2) Faculty mentor name: Prof. Alexei Orlov
3) Project title: Nanoelectronic material characterization using single electron transistors

4) Briefly describe any new skills you acquired during your summer research:

I first learned how to safely work in the cleanroom. This includes distinguishing the uses of different hoods, chemical disposal, and emergency preparedness. After this training, I was trained on the spinner and hotplate bench and the OAI system for photolithography. This training would then prove useful in printed circuit board fabrication. Additionally, I received training on the MOS-FET clean bench and the furnace which are used in wafer fabrication. I have also learned how to use a probe card station and accompanying semiconductor parameter analyzer. Lastly, I learned to use CAD software to design circuit boards.

5) Please briefly share a practical application/end use of your research: The MOS transistor has become incredibly small since its innovation. As the title of the project suggests, it is now possible to fabricate single electron transistors. However, these are not yet used in industry as it is hard to tell whether or not regular MOS transistors of this size are defective. Fortunately, it may be possible to quickly tell if a transistor is defective or not by first characterizing the properties of working single electron transistors.

Project summary:

Misplacing a few dopants within a single electron transistor can be extremely damaging to its performance due to the devices small size. Thus, it is important to be able to recognize defective transistors and to develop tests that indicate imperfections in the devices. To do this electronic materials are introduced into the structure of the single electron transistors. These additional materials allow for evaluation of defects in a transistor. Once a transistor is fabricated with these materials, conductance mapping and microwave reflectometry are used to characterize the properties of the transistor. Based on the results, defects in a transistor can be recognized based on the observed properties of the transistors structure.

The objective of the summer is to prepare the hardware for an upcoming experiment. In part of the setup a break-out box is needed to interface with a probe-card station. Thus, I created a cable that connects a DB50 serial port to the probe-card station. Afterwards, the need for a panel to hold phase shifters and attenuators was recognized. As such, I designed the aforementioned panel which will allow for adjustments to be made to the experiment's parameters. Lastly, the output of the experiment is taken in the form of a small AC voltage. To make a proper measurement of the output, a circuit to accurately measure the RMS value of an AC voltage was needed. This circuit would rectify the signal, filter the rectified signal to remove the AC components of the rectified signal so that the output would become a clean DC signal; the additional amplification was necessary to raise the level of signal to the levels suitable to a digitizer with a 10V full scale. After designing the circuit, and laying out the printed circuit

board using Eagle © Printed circuit boards design software, photolithography was used to fabricate the circuit. Then the gain of the circuit and the cutoff frequency was then adjusted so that it met the parameters needed in the experiment. Next, the performance of the circuit was evaluated using a SRS830 lock-in amplifier and a BK2706A digital multimeter. The two attached plots demonstrate the DC response to a 1.3 kHz sinusoidal signal where linear dependence is clearly seen, and frequency dependence of the circuit response to a sinusoidal signal with RMS value of 196 mV, which demonstrates that the circuit works fine in the range 40Hz -80kHz.

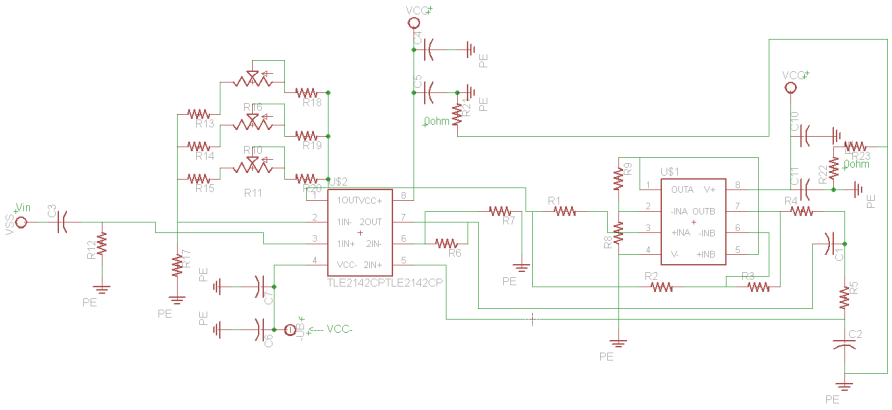

Figure 1-Absolute Value Circuit Schematic

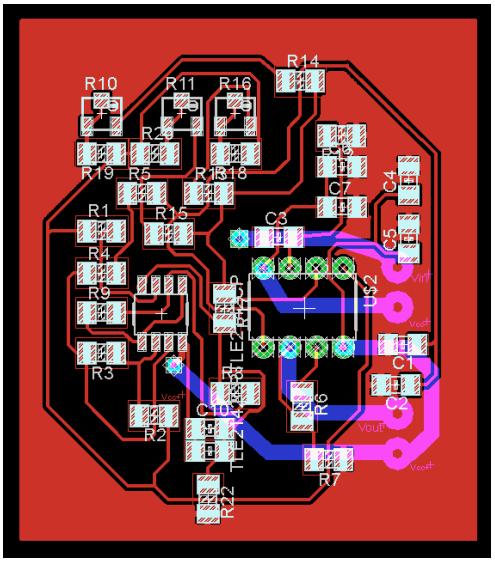

Figure 2-Absolute Value Circuit PCB Layout

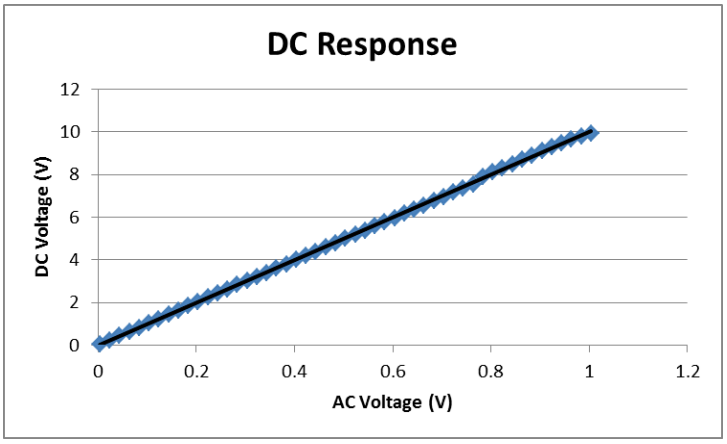

Figure 3-DC Response Graph

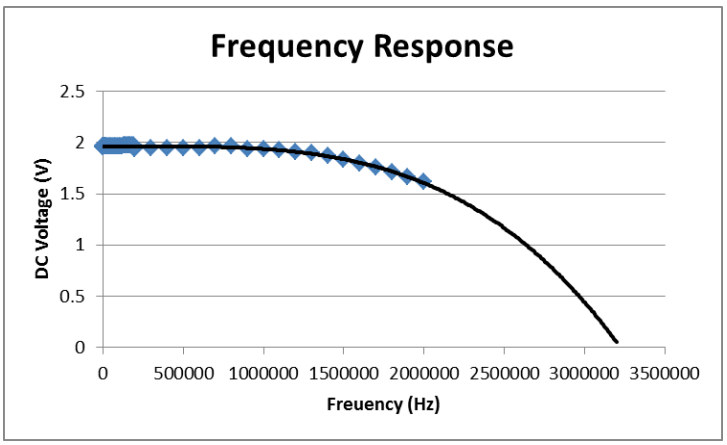

Figure 4 - Frequency Response Graph