NDnano UNIVERSITY OF NOTRE DAME CENTER FOR NANO SCIENCE AND TECHNOLOGY

ND*nano* Undergraduate Research Fellowship (NURF)
2013 Project Summary

1) Student name: Jung Whan (Stephen) Kim
2) Faculty mentor name: Alan Seabaugh, Patrick Fay (project advisor)
3) Project title: Electrical characterization of silicon-on-insulator substrates – SunEdison project

4) Briefly describe any new skills you acquired during your summer research:

1. Network analyzer 8722D (high frequency: 100 MHz – 40 GHz), network analyzer 8753E (low frequency: 30 kHz – 6 GHz)
- SOLT (Short, Open, Load, Through) calibration: Calibration was done by obtaining 10 independent data (open, short, resistance, and through with reflection and transmission from the port 1 and port 2).
- Two network analyzers with different frequency ranges were used to understand the S parameter behaviors at low and high frequency range.

2. Impedance analyzer Cascade Microtech Summit 11861 Prober
- Calibration: Calibration was done by following the steps in the manual.
- It was used to understand the CV characteristics of the fabricated samples.

3. ADS
- The program was used to plot the S parameter data.
- The fabricated samples' magnitude and phase of S parameters, characteristic impedance (Zo), and attenuation coefficient plots were used to determine the wafer with trap charge density which minimizes the RF loss.

4. KaleidaGraph
- The program was used for the TFET modeling and data analysis.

5) Please briefly share a practical application/end use of your research:

The goal of this project was to study the characteristics of HR-SOI wafers with the silicon interface trap charge density. For the 10 week project, Dr. Seabaugh's research group fabricated and collected the data to understand the effect of the silicon interface trap charge density on RF loss. The project addressed the issues which SunEdison has faced with its commercial HR-SOI wafers. Dr. Seabaugh's group and SunEdison will continue to collaborate on studying the issues with HR-SOI wafers in the upcoming semester and I'll continue to work on the measurements of the fabricated samples with a new structure.

Project summary:

Dr. Seabaugh's research group collaborated with SunEdison, a semiconductor and solar cell manufacturer, to evaluate the RF loss for 4 wafers with different trap charge density. Sushant Sabnis, a graduate student at Notre Dame, fabricated the 6 CPW samples on 1 Control and 3 Sample wafers with different trap charge density. Based on these 6 samples, I focused on the S parameter and CV characteristics data measurement and analysis.

First, we simulated and set the dimensions of the coplanar waver guide lines based on the characteristic impedance calculated from the equations in the waveguide book (Reference Data for Radio Engineers: Radio, Electronics, Computer, and Communications, 7th edition, Ed. By C. Jordan, pp. 29-26-29-27 (1985). The Figure 1 is the mask design for fabrication. It contains the coplanar waveguide lines with 5 different lengths (.5, 1, 2, 4, 8 mm). It also has a variation of the gap w, distance between the center conductor line and the two ground lines next to it (25, 30, 35, 40, 45 μm). The variations in length and gap were used to understand the change in S parameter characteristics. The dots at the bottom of the mask design were used for the CV characteristic measurements.

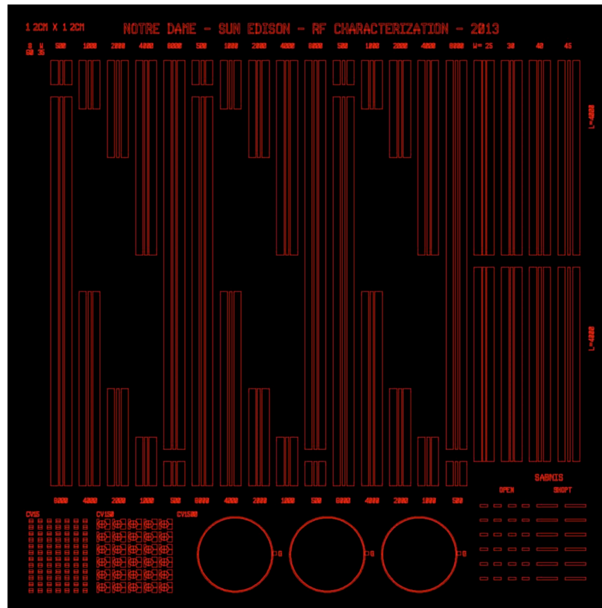

Figure 1. Mask design – The waveguide lines with 5 different lengths: 0.5, 1, 2, 4, 8 mm. w (gap between the center waveguide and the two lines next to it) is fixed (35μm). For the width variation (25, 30, 35, 40, and 45μm), s is fixed (60μm).

Based on the mask design, Sushant fabricated 6 different samples on the wafers provided by SunEdison. The wafer type, date, and thickness of the metal used for the waveguide lines, and comments are summarized in the table below. The network analyzers were used to characterize the S parameters for each sample. To study the effect of the different trap charge density, C1D1, S1A1, S2A1, and S3A1 were used for the data comparison.

Sample	Wafer	Die	Date	Metal	Thickness (nm)	Comments
C1	A3		6/23/13	Al	250	back oxide removed
C1	A2		7/2/13	Ti/Au	5/245	stepper
S3	A1		7/9/13	Ti/Au	5/245	stepper
C1	D1	1,2	7/29/13	Ti/Au	5/245	contact lithography
S1	A1	1,2,3,4	7/30/13	Ti/Au	5/245	contact lithography
S2	A1	1,2,3,4	7/30/13	Ti/Au	5/245	contact lithography

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Figure 2. Summary of the fabrication process.

Three types of measurements were done in a network analyzer: S parameter data without dc bias at high frequency range (100 MHz - 35 GHz with), S parameter data without dc bias at low frequency range (30 kHz – 2 GHz), and S parameter data with dc bias (-5 to 5V with 0.2V step size) at low frequency range. To understand the variations in RF loss of the 1 Contol and 3 Sample wafers with different trap charge density, we studied the magnitude and phase of S Parameter data, characteristic impedance, attenuation coefficient at low and high frequency ranges with and without the dc bias, light dependence on attenuation coefficient, and comparison with the data from the reference papers. Dr. Seabaugh's group and SunEdison have not made a conclusion on the effect of different trap charge density and there will be more data measurements and analysis to understand the effect in the upcoming semester.

Publications (papers/posters/presentations): PowerPoint slides were presented to SunEdison, but we are allowed to share the data only with the company.