UNIVERSITY OF NOTRE DAME
NDnano
CENTER FOR NANO SCIENCE AND TECHNOLOGY

Nanoelectronics Undergraduate Research Fellowship (NURF) 2010 Project Summary

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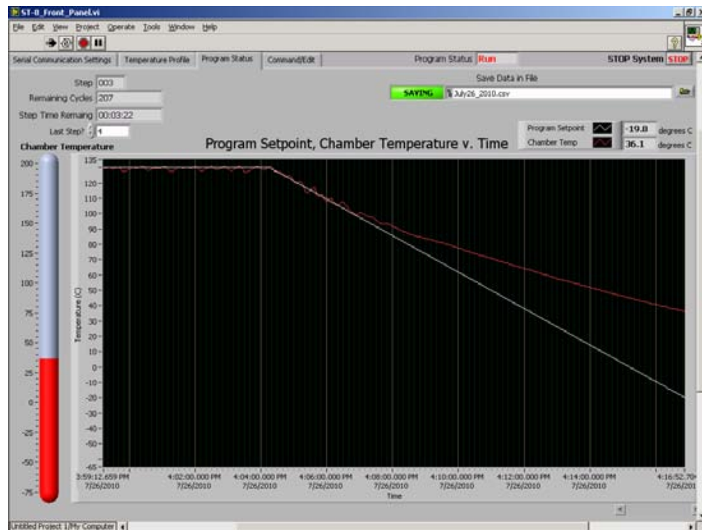
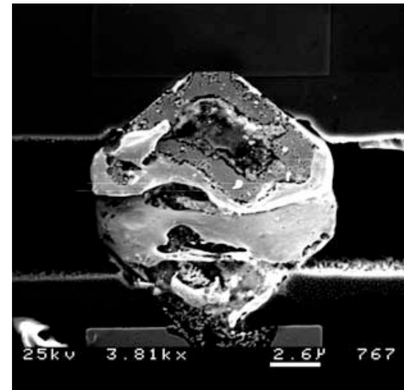
Faculty mentor name: Dr. Gary H. Bernstein
Project title: Thermal Reliability of Quilt Packaging

In order to validate the viability of novel interconnect technology, Quilt Packaging, it must be subject to the same reliability standards as other technologies. My project was to enable our lab to perform in-house thermal stress tests of ‘quilted’ chips so that simulations of different nodule designs could be checked against experimental results.

To accomplish this, the lab purchased an Envirotronics ST-8 temperature chamber, capable of temperatures from -70 C to 160 C. The chamber functioned well, but had extremely limited data readout. The chamber had a serial port for remote operation, so I used National Instruments’ LabVIEW to create a more useable interface and save the temperature profile to an Excel file for easier analysis. I also worked to solder a few pairs of chips together, image the connections using an SEM and begin temperature cycling tests per the JEDEC standard JESD22-A104D. At the time of writing, the first sample had undergone 325 cycles and the second sample 71 cycles of 500 cycles until first inspection.



LabVIEW interface to ST-8 temperature chamber



SEM image of soldered nodules before testing

The poster “Thermal Reliability of Quilt Packaging Interconnects” will be presented.